REMARKS

I. General

Claims 1-13 are pending in the present application.

The specification was objected to because the section "Brief Description of the Drawings" is missing.

Claim 12 was objected to because of informality.

Claims 1-13 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Momtaz et al. (US7,263,151) in view of Moll et al. (US 7,069,488).

Claims 12 has been amended as suggested by the Examiner.

II. Objection of the Specification

The specification was objected to because the section "Brief Description of the Drawings" is missing. By this response, the specification has been amended to include the missing section.

III. Objection of Claim 12

Claim 12 was objected to because it is deemed that a "product" is structural and it is not possible to encode a structure into a readable medium. Claim 12 has been amended to remove the word "product" as suggested by the Examiner.

IV. Rejection of Claims 1-13 under 35 U.S.C. § 103(a) as being unpatentable over Momtaz et al. (US7,263,151) in view of Moll et al. (US 7,069,488)

Claims 1 and 10

It is stated in the Office Action that Applicants' arguments submitted on July 14, 2008 have been considered but are moot in view of the new grounds of rejection. In the earlier Final Action, it was cited that a number of elements of Claim 1 are disclosed in Momtaz. Applicants have traversed by showing that such is not the case previously, but the Examiner repeated the

same anticipation by Momtaz in the current Office Action without answering the substance of Applicants' traversal. Should the Examiner continue to repeat this rejection after this reply, Applicants respectfully request that the Examiner answer all material traversed as required by MPEP 707.07(f) which states that "where the Applicant traverses any rejection, the Examiner should, if he or she repeats the rejection, take note of the applicant's argument and answer the substance of it".

In the Office Action, Claims 1 and 10 have been rejected as being obvious and therefore unpatentable over Momtaz in view of Moll. Specifically, it is cited in the Office Action that Momtaz discloses the level comparator, the sampling unit and the bit error test unit recited in Claim 1 but does not disclose "comparing the sampled comparator output signal against an expected pattern" performed by the bit error test unit.

In response to this rejection, Applicants respectfully but strongly submit that the reference disclosures, Momtaz and Moll, do not render Applicant's invention according to Claim 1 and 10 obvious. Specifically, Applicants submit that Momtaz does not anticipate a number of Applicants' elements and, in particular, the manner in which these elements are connected to each other as recited in Claim 1. Applicants also submit that there is no motivation for one ordinarily skilled in the art to combine the teachings of Momtaz and Moll.

Since there is no answer in the Office Action to Applicants' previously submitted traversal, Applicants repeat the arguments previously submitted to show that Momtaz does not anticipate a number of features of Applicants' Claim 1. Applicant's Claim 1 recites "a sampling unit coupled to the level comparator and being adapted for sampling the comparator output signal". That is, Applicants' sampling unit is connected to the level comparator and is used to sample an output signal of the level comparator. Applicants submit that Momtaz does not disclose, teach or suggest any sampling unit that is used to sample an output signal of a level comparator.

The cited col. 8, lines 50-56 of Momtaz discloses "a comparator having a first input coupled to an output of the integrator and a second input coupled to a threshold voltage, wherein the delay circuit is configured to shift the phase of the incoming data signal in a manner that is symmetrical with respect to a sampling edge of the clock signal". The comparator's output is a statistical loss of signal (SLOS) signal. (See col. 4, lines 20-22 and Figure 1 of Momtaz.) The clock signal is however applied to a flip-flop which is not connected to the comparator. (See col.

2, lines 35-52 and Figure 1 of Momtaz.) The flip flop therefore does not sample the SLOS signal at the output of the comparator. The flip flop is merely used to latch the clock signal using delayed data. (See col. 4, lines 38-39 and Figure 2 of Momtaz.) Therefore, unlike Applicants' sampling unit that is connected to the level comparator to sample the output signal of the comparator as recited in Claim 1, Momtaz's flip-flop does not even sample the SLOS signal let alone "sample the comparator output signal" as recited in Applicant's Claim 1. In other words, Momtaz does not disclose Applicants' sampling unit and, especially, a sampling unit that is connected to the level comparator in a manner as recited in Claim 1.

In this reply, Applicants submit that Claim 1 further recites "a bit error test unit adapted to receive the sampled comparator output signal and to determine therefrom an indication of a bit error in a sequence of the sampled comparator output signal by comparing the sampled comparator output signal against an expected pattern." Applicant submits that Momtaz does not disclose any such bit error test unit that is connected to the sampling unit to receive the sampled comparator output signal of the sampling unit. The cited passage (Col. 3, lines 1-12) in Momtaz merely discloses various components that are able to provide a bit error rate of the incoming signal; none of which is a bit error test unit as recited in Claim 1. Accordingly, it is correctly stated in the Office Action that Momtaz "fail[s] to teach comparing the sampled comparator output signal against an expected pattern" since Momtaz does not disclose such a bit error test unit.

Turning to the combination of the teachings of Momtaz and Moll, Applicants submit that there is no reason for a person having ordinary skill in the art to incorporate Moll's teaching of "comparing the sampled comparator output signal against an expected pattern" into Momtaz's receiver, in light of the teaching of Momtaz.

It is cited in the Office Action that "a deviation in the corresponding samples would indicate error in the signal" and "therefore, accurate analysis of the signal would be performed."

Applicants submit that Momtaz's loss-of-signal detector is used in a telecommunication application that is "not limited to any specific telecommunication standard" (see Col. 4, lines 28-34). Therefore, since the loss-of-signal detector can be used in any telecommunication standard, data received by the loss-of-signal detector is unknown to the loss-of-signal detector. And since the data received is unknown, the loss-of-signal detector does not know what data to expect and therefore cannot compare the data received with any expected pattern. It is precisely because of

this unknown data that the principle of operation of Momtaz's loss-of-signal detector's is based on "comparing phase of the clock signal extracted from the incoming data with that of a delayed version of the incoming data. The results of this comparison are averaged over time to arrive at the BER. The measured BER is compared to a pre-determined threshold value to detect a loss-of-signal condition." See col. 2, lines 11-20 of Momtaz. Since data received is unknown, the detector does not know what data to expect and so it only compares the phase of the clock signal extracted from the incoming data with the phase of a delayed version of the incoming data. Only phases of signals external to the loss-of-signal detector are compared; there is no comparison of any signal against an expected pattern. Modifying Momtaz's loss-of-signal detector by adding Moll's teaching of "comparing the sampled comparator output signal against an expected pattern" **serves no purpose** as the loss-of-signal detector does not know what signal pattern to expect. Therefore, one ordinarily skilled in the art would not make such a modification.

Furthermore, **if** the loss-of-signal detector knows what data (signal) to expect and is able to compare the data received with expected data to provide "accurate analysis of the signal", that would render the SLOS feature of Momtaz's invention redundant. If an accurate analysis of the signal is available, there will no longer be any need for the SLOS block since information obtained from such a block can be directly and accurately obtained from that comparison that provides the "accurate analysis". That would change the principle of operation of Momtaz, and the teachings of Momtaz and Moll are thus not sufficient to render Claim 1 obvious. (See MPEP 2143.01 VI.)

Momtaz also discloses the need to minimize capacitive loading on the data line and clock line introduced by the loss-of-signal circuitry. The circuitry only adds the capacitive loading of a single flip-flop to the recovered clock line, while it capacitively loads the data line by no more than the delay circuit. (See abstract, col. 2, lines19-23 and lines 30-34,.) To carry out any accurate analysis of the signal as suggested by the Examiner, additional circuitry will have to be connected to the data line and the recovered clock line of Momtaz where only the data and clock are available. Such an incorporation of additional circuitry will undoubtedly introduce further capacitive loading which may render the modified circuit unacceptable in the 10 GHz and above frequency range as disclosed in col. 3, lines 58-65 of Momtaz. Momtaz therefore teaches away from adding additional circuitry to its loss-of-signal detector and especially the feature of Moll since it serves no purpose as explained above.

In view of the foregoing, it is submitted that Claims 1, and Claim 10 having subject matter similar to that of Claim 1, are allowable. For the same reasons, it is submitted that Claims 2-9 and 11, which variously depend from Claim 1 and Claim 10 respectively, are also allowable. However, some of these claims are allowable for the following additional reasons.

Claim 2

Claim 2 recites "a phase shifting unit being adapted to receive and phase-shift a clock signal and to provide to the sampling unit a phase-shifted clock signal for controlling a sampling point of the sampling unit." Col. 2, lines 35-53 of Momtaz however discloses a delay circuit that is configured to shift a phase of the incoming data signal. That is, the delay circuit in Momtaz does not anticipate the phase-shifting of the clock signal as recited in Claim 2.

Claim 3

Claim 3 recites "a control unit being adapted to control the comparison level of the level comparator." On the other hand, the comparator, and thus the threshold voltage V_{TH} thereof, in Momtaz is not controlled.

Claim 4

Applicants submit that it is not clear what in Momtaz constitutes Applicants' control unit. If the clock and data recovery (CDR) block and the retimer in Momtaz are considered to anticipate Applicants' control unit, the CDR block and the retimer are not controlled at all, much less, by at least one of the bit error test unit and an interface unit adapted to be coupled to a unit external with respect to the integrated circuit as recited in Claim 4.

Claim 5 and Claim13

Claim 5 recites "an input unit adapted to receive an input signal from external with respect of the integrated circuit" and the input unit includes the level comparator and the sampling unit. The level comparator receives the input signal as the comparator input signal. The comparator in Momtaz however receives a signal output from an integrator. The output of the integrator is not an input signal external to Applicants' integrated circuit.

The integrated circuit may also include "a processing unit adapted to receive and process the sampled comparator output signal" and "an output unit adapted to receive a data signal from

the processing unit, to derive therefrom an output signal, and to provide the output signal to external with respect of the integrated circuit". Momtaz does not disclose any processing unit or output unit. For the same reason, Claim 13 which is the combination of the subject matter of Claim 1 and Claim 5 is also allowable.

Claim 9

Claim 9 recites "the sampling unit comprises a deserializer adapted for deserializing the comparator output signal". This deserializer deserializes the high speed comparator output signal COS to a lower speed signal. (See para [28].) Again, Momtaz does not disclose such a deserializer. The cited SONET OC-192 application is not part of Momtaz's loss-of-signal detector. The cited passage (col. 4, lines 25-38) merely discloses that Momtaz's loss-of-signal detector receives a 10Gb/s incoming data and a 10GHz extracted clock signal from a SONET OC-192 application.

CONCLUSION

In view of the discussions set forth herein, it is respectfully submitted that the grounds for the Examiner's objections and rejections have been overcome. Accordingly, it is respectfully submitted that Claims 1-13 should be found to be in condition for allowance.

Respectfully submitted,

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Dated: January 1, 2009

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